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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,945	03/30/2004	Douglas Glenn Wildes	134730	5777

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EXAMINER	
ZARROLI, MICHAEL C	

ART UNIT	PAPER NUMBER
2839	

DATE MAILED: 04/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,945	WILDES ET AL.	
	Examiner	Art Unit	
	Michael C. Zarroli	2839	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-20 and 30-33* is/are allowed.

6)☒ Claim(s) *1,3-4,6,9,21-25,27-28,* is/are rejected.

7)☒ Claim(s) *2,5,7,8,26 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/22/04,3/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1, 21 and 27 objected to because of the following informalities: These claims should be paragraphed for easier understanding. Appropriate correction is required.

2. Claims 28 objected to because of the following informalities: In line 3 shouldn't "third and fourth circuit boards" be –third and fourth stacked connections--? Appropriate correction is required.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the an alignment pin anchored in a first spacer and projecting through openings in circuit boards of the second stacked connection and into a hole in the second spacer must be shown or the feature(s) canceled from the claims 27-29 (see obviousness rejection of claim 27). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on

the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3-6 and, 9 rejected under 35 U.S.C. 102(b) as being clearly anticipated by Carson et al.

Carson et al discloses a stacked connection (title) comprising first, second and third circuit boards (fig. 11) having respective overlapping portions, said first circuit board (top layer) comprising a substrate supporting first (82,1st) and second (88,1st) sets of electrical conductors, said second circuit board (next layer below top or first) comprising a substrate supporting first (88,2nd) and second (86,2nd) sets of electrical conductors, and said third circuit board (bottom of the staggered boards parallel to 83) comprising a substrate supporting a first set of electrical conductors (88,3rd), wherein said second set of electrical conductors (86,2nd) of said second circuit board are respectively in contact with said second set of electrical conductors (88,1^{st}) of said first circuit board, and said first set of electrical conductors (88,3^{rd}) of said third circuit board are respectively electrically coupled (by way of 81) to said first set of electrical conductors (82,1^{st}) of said first circuit board by way of said first set of electrical conductors (88,2^{nd}) of said second circuit board.

Regarding claim 3 Carson discloses that a first portion of said second circuit board is bonded to a portion of said first circuit board, and a portion of said third circuit board is bonded to a second portion of said second circuit board (fig. 11).

Regarding claim 4 Carson discloses that a first portion of said second circuit board is soldered to a portion of said first circuit board, and a portion of said third circuit board is soldered to a second portion of said second circuit board (col. 3 lines 40-50).

Regarding claim 5 Carson discloses that a clamp clamps said first through third circuit boards together (fig. 3).

Regarding claim 6 Carson discloses that said third circuit board further comprises a second set of electrical conductors supported by said substrate of said third circuit board, further comprising a fourth circuit board, said fourth circuit board comprising a substrate supporting a set of electrical conductors, wherein said set of electrical conductors of said fourth circuit board are respectively electrically coupled to said first set of electrical conductors of said first circuit board by way of said first sets of electrical conductors of said second and third circuit boards connected in series (fig. 11 *shows a fourth circuit board with similar connections*).

Regarding claim 9 Carson discloses that the ends of said second and third circuit boards remote from said first circuit board are embedded in a body of acoustically attenuative material (figures 9 & 11).

6. Claims 21-23 rejected under 35 U.S.C. 102(b) as being clearly anticipated by Tai et al.

Tai discloses an apparatus comprising first and second stacked connections (fig. 3 right & left sides) and a spacer (200) disposed between said first and second stacked connections, said first stacked connection comprising first and second circuit boards (unnumbered fig. 3), said second stacked connection comprising third and fourth circuit boards (unnumbered fig. 3), wherein said spacer comprises a first set of electrical conductors (C1...4 & 210), said first circuit board comprises a second set of electrical conductors (B24), and said fourth circuit board comprises a third set of electrical conductors (B44), said electrical conductors of said second set being respectively electrically connected to said electrical conductors of said third set by way (see fig. 3) of said electrical conductors of said first set.

Regarding claim 22 Tai discloses that said second circuit board (fig. 3 at 20A) is disposed between said first circuit board and said spacer, wherein said second circuit board comprises a fourth set of electrical conductors (B14), said electrical conductors of said second set (B24) being respectively electrically connected to said electrical conductors of said first set (C1...4 & 210) by way of said electrical conductors of said fourth set (electrical connection between first and second circuit boards by way of L14 & T14).

Regarding claim 23 Tai discloses that within each of said first and second stacked connections the circuit boards are bonded together (figures 3 & 4).

Claim Rejections - 35 USC § 103

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 24 rejected under 35 U.S.C. 103(a) as being unpatentable over Tai et al as applied to claim 21 above, and further in view of Nishiuma et al.

Tai does not disclose that the circuit boards are soldered together.

Nishiuma discloses soldering circuit boards together in a stack (col. 6 line 20).

At the time the invention was made it would have been obvious to one of ordinary skill in the art to bond the circuit boards of Tai together with solder as taught by Nishiuma. The suggestion for this is found in Tai where Tai says that the circuit boards are bonded together. Bonding could imply soldering.

10. Claim 25 rejected under 35 U.S.C. 103(a) as being unpatentable over Tai et al as applied to claim 21 above, and further in view of Farnworth.

Tai does not disclose that the circuit boards and spacer together.

Farnworth discloses circuit boards and a spacer held together with a clamp (fig. 6).

At the time the invention was made it would have been obvious to one of ordinary skill in the art to hold the circuit boards and spacer of Tai together with a clamp as taught by Farnworth. The motivation for this would be to allow for easy disassembly.

11. Claims 27-28 rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano in view of Tamarkin et al.

Nakano discloses an apparatus comprising first, second and third stacked connections (various figures), a first spacer (fig. 2 at 24 & 25) disposed between said first and second stacked connections, and a second spacer (fig. 2 at 53 & 54) disposed between said second and third stacked connections, each of said first, second and third stacked connections comprising a respective plurality of circuit

boards (e.g. fig. 6 at 10, 20, 30 & 40), wherein said second spacer comprises a hole (fig. 4) and each circuit board of said second stacked connection comprises a respective opening (figures 4 & 12), further comprising a first alignment pin (10b) anchored in said first spacer and projecting through said openings in said circuit boards of said second stacked connection and into said hole in said second spacer (figure 12 or maybe figure 17).

Nakano does not specifically show three stacks of multiple circuit boards (CB) each separated by two spacers (Sp); an CB-Sp-CB-Sp-CB relationship.

Similarly for claim 28 Nakano does not specifically show four stacks of multiple circuit boards (CB) each separated by two spacers (Sp); an CB-Sp-CB-Sp-CB-Sp-CB relationship.

Tamarkin discloses a CB-Sp-CB-Sp-CB relationship of stacked connectors (fig. 1).

At the time the invention was made it would have been obvious to one of ordinary skill in the art to arrange the stacked connections and spacers of Nakano in the CB-Sp-CB-Sp-CB setup of Tamarkin. The suggestion for this is found in Nakano where various arrangements are suggested. Well-settled case law has shown that merely shifting the location of parts is not grounds for a patent *In re Japiske, 181 F.2d 1019, 102, 86 USPTQ 70, 73 (CCPA 1950*

Regarding claim 28 it would have been obvious to one of ordinary skill in the art to arrange the stacked connections and spacers of Nakano in the CB-Sp-CB-Sp-CB-Sp-CB relationship. The motivation fro this would be to increase functionality of the device. Duplicating parts for a multiple effect is not in and of itself grounds for a patent *In re Harza, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960).*

Allowable Subject Matter

12. Claims 10-20 and, 30-33 allowed over the prior art of record.

13. Claims 2, 5, 7-8, 26 and, 29 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tukamoto et al teaches stacked groups of circuit boards with spacers. Eng et al teaches stacks of circuit boards and alignment pins.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Zarroli whose telephone number is 571-272-2101. The examiner can normally be reached on 7:30 to 3:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, T.C. Patel can be reached on (571) 272-2800 ext 39. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael C. Zarroli
Primary Examiner
Art Unit 2839

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